AMENDMENTS TO THE DRAWINGS

Fig. 2D is objected to as its replacement sheet was not properly labeled. A properly labeled replacement sheet for Fig. 2D is submitted herewith.

Figs. 1A and 1B are objected to as missing labels for elements 100 through 112 and including confusing references to the number of bits. Figs. 1A and 1B are amended herewith to correct these defects.

Fig. 5C is objected to as missing description for elements 514 and 516. Fig. 5C is amended herewith to correct these defects.

REMARKS

The present response is intended to be fully responsive to all points of rejection raised by the Examiner in the Office Action dated February 26, 2007, and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

DRAWING OBJECTIONS

Fig. 2D is objected to as its replacement sheet was not properly labeled. A properly labeled replacement sheet for Fig. 2D is submitted herewith.

Figs. 1A and 1B are objected to as missing labels for elements 100 through 112 and including confusing references to the number of bits. Figs. 1A and 1B are amended herewith to correct these defects.

Fig. 5C is objected to as missing description for elements 514 and 516. Fig. 5C is amended herewith to correct these defects.

CLAIM REJECTIONS

35 U.S.C. § 102(e) Rejections

Claims 1 – 7, 9 – 18, 20 – 29, and 31 – 33 have been rejected under 35 U.S.C. §102(e), as being anticipated by U.S. Patent Application Publication No. 2005/0055536 to Ansari (hereinafter "Ansari"). Applicant respectfully traverses this rejection in view of the remarks that follow.

Ansari describes prefetching and loading data into vector registers and uses the term "vectors" to refer to blocks of data that are being prefetched. Where prefetched data resides in non-contiguous locations in memory ("the stride between the data elements is larger than one") Ansari describes packing several memory elements together in order to make more efficient use of the memory bus. Ansari therefore refers only to efficient transferring of data between memory and a vector file.

The present invention teaches how to take advantage of a vector register file in a Single Instruction Multiple Data (SIMD) processor architecture and indirection to reorder data in support of the operations that are performed upon the data, and not when reading/writing the data from/to memory. While Ansari relates to efficient transfer of

data between memory and the processor, the present invention relates to activities performed in support of the computation itself, including handling permutations, alignment, and parametric permutations.

While both the present invention and Ansari use the term "vector," they nevertheless relate to two different things. In Ansari, a vector is a contiguous block in memory or in a buffer, whereas in the present invention a vector refers to the data source and destination of SIMD instructions. In the present invention the term "vectorization" refers to transforming a sequence of program instructions that work on single elements (scalar) into instructions that work on compound elements (vector) while preserving the program semantics. Because each instruction operates on several elements, performing the vectorization of the present invention results in faster executed. However, as not all program elements are amenable to such transformations, the present invention provides for identifying instruction sequences within a program that are transformable. Ansari does not relate at all to transforming program instructions to take advantage of processor architectures that enable parallel execution, and only refers to transferring of data to and from main memory.

Claim 1 is amended herewith to better distinguish the claimed invention from the prior art, where:

- the terms "vectorization" and "vectorizable" have been replaced with their underlying definitions as described in the specification;
- the claimed invention is limited to architectures that support SIMD parallel execution, and;
- the claimed invention uses an indirect addressing vector pointer register that is configured into a multiport, scalar register file containing independently addressable elements.

Applicant respectfully submits that claim 1, as amended, is not anticipated by Ansari which lacks these features. Applicant respectfully requests, therefore, that the rejection of claim 1 under 35 U.S.C. § 102(e) be withdrawn.

Claims 2 – 7 depend directly or indirectly from independent claim 1, and are, *a fortiori*, deemed allowable in view of the discussion above with regard to claim 1. Applicant respectfully requests, therefore, that the rejection of claims 2 – 7 under 35 U.S.C. § 102(e) be withdrawn.

Claim 9 is amended herewith to include the limitations of claim 1 as discussed above and is likewise not anticipated by Ansari. Applicant respectfully requests, therefore, that the rejection of claim 9 under 35 U.S.C. § 102(e) be withdrawn.

Claims 10 and 11 depend directly or indirectly from independent claim 9, and are, *a fortiori*, deemed allowable in view of the discussion above with regard to claim 1. Applicant respectfully requests, therefore, that the rejection of claims 10 and 11 under 35 U.S.C. § 102(e) be withdrawn.

Claim 12 is amended herewith to include the limitations of claim 1 as discussed above and is likewise not anticipated by Ansari. Applicant respectfully requests, therefore, that the rejection of claim 12 under 35 U.S.C. § 102(e) be withdrawn.

Claims 13 – 18 depend directly or indirectly from independent claim 12, and are, *a fortiori*, deemed allowable in view of the discussion above with regard to claim 1. Applicant respectfully requests, therefore, that the rejection of claims 13 – 18 under 35 U.S.C. § 102(e) be withdrawn.

Claim 20 is amended herewith to include the limitations of claim 1 as discussed above and is likewise not anticipated by Ansari. Applicant respectfully requests, therefore, that the rejection of claim 20 under 35 U.S.C. § 102(e) be withdrawn.

Claims 21 and 22 depend directly or indirectly from independent claim 20, and are, *a fortiori*, deemed allowable in view of the discussion above with regard to claim 1. Applicant respectfully requests, therefore, that the rejection of claims 21 and 22 under 35 U.S.C. § 102(e) be withdrawn.

Claim 23 is amended herewith to include the limitations of claim 1 as discussed above and is likewise not anticipated by Ansari. Applicant respectfully requests, therefore, that the rejection of claim 23 under 35 U.S.C. § 102(e) be withdrawn.

Claims 24 – 29 depend directly or indirectly from independent claim 23, and are, *a fortiori*, deemed allowable in view of the discussion above with regard to claim 1. Applicant respectfully requests, therefore, that the rejection of claims 24 – 29 under 35 U.S.C. § 102(e) be withdrawn.

Claim 31 is amended herewith to include the limitations of claim 1 as discussed above and is likewise not anticipated by Ansari. Applicant respectfully requests, therefore, that the rejection of claim 31 under 35 U.S.C. § 102(e) be withdrawn.

Claims 32 and 33 depend directly or indirectly from independent claim 31, and are, *a fortiori*, deemed allowable in view of the discussion above with regard to claim 1. Applicant respectfully requests, therefore, that the rejection of claims 32 and 33 under 35 U.S.C. § 102(e) be withdrawn.

35 U.S.C. § 103(a) Rejections

Claims 8, 19, and 30 have been rejected under 35 U.S.C. §103(a), as being unpatentable over U.S. Patent Application Publication No. 2005/0055536 to Ansari in view of U.S. Patent No. 6,446,105 to Washio, et al. While Applicant respectfully traverses this rejection, claims 8, 19, and 30 depend directly or indirectly from independent claims 1, 12, and 23 respectively, and are, *a fortiori*, deemed allowable in view of the discussion above with regard to claim 1. Applicant respectfully requests, therefore, that the rejection of claims 8, 19, and 30 under 35 U.S.C. § 103(a) be withdrawn.

Conclusion

Applicant respectfully submits that consideration of the above remarks renders the present application in condition for allowance, which action Applicant respectfully solicits.

Favorable action on this response is courteously solicited.

Please charge any fees associated with this response to Deposit Account 09-0468.

Respectfully submitted,

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